SE97

Memory module temp sensor with integrated SPD

Rev. 02 — 12 October 2007 Product data sheet

1. General description

The NXP Semiconductors SE97 measures temperature from −40 °C and +125 °C and also provides 256 bytes of EEPROM memory communicating via the I²C-bus/SMBus. It is typically mounted on a Dual In-Line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Temperature Sensor Component* specification and also replacing the Serial Presence Detect (SPD) which is used to store memory module and vendor information.

Placing the Temp Sensor (TS) on a DIMM allows accurate monitoring of the DIMM module temperature to better estimate the DRAM case temperature (T_{case}) to prevent it from exceeding the maximum operating temperature of 85 °C. The chip set throttles the memory traffic based on the actual temperatures instead of the calculated worst-case temperature or the ambient temperature using a temp sensor mounted on the motherboard. There is up to 30 % improvement in thin and light notebooks that are using one or two 1 GB SO-DIMM modules, although other memory modules such as in server applications will also see an increase in system performance. Future uses of the TS will include more dynamic control over thermal throttling, the ability to use the Alarm Window to create multiple temperature zones for dynamic throttling and to save processor time by scaling the memory refresh rate.

The TS consists of a ΔΣ Analog to Digital Converter (ADC) that monitors and updates its own temperature readings 10 times per second, converts the reading to a digital data, and latches them into the data temperature register. User-programmable registers, the specification of upper/lower alarm and critical temperature trip points, $\overline{\text{EVENT}}$ output control, and temperature shutdown, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE97 outputs an $\overline{\text{EVENT}}$ signal using an open-drain output that can be pulled up between 0.9 V and 3.6 V. The user has the option of setting the $\overline{\text{EVENT}}$ output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The $\overline{\text{EVENT}}$ output can even be configured as a critical temperature output.

The EEPROM is designed specifically for DRAM DIMMs SPD. The lower 128 bytes (address 00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. This allows DRAM vendor and product information to be stored and write protected. The upper 128 bytes (address 80h to FFh) are not write protected and can be used for general purpose data storage.

The SE97 has a single die for both the temp sensor and EEPROM for higher reliability and supports the industry-standard 2-wire I²C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identity of the device. Three address pins allow

up to eight devices to be controlled on a single bus. To maintain interchangeability with the I²C-bus/SMBus interface, the electrical specifications are specified with the operating voltage of 3.0 V to 3.6 V.

DIMM applications normally use the C-grade accuracy SE97PW or SE97TK temp sensor. For applications requiring the higher B-grade accuracy, the SE97PW/1 or SE97TK/1 is available.

2. Features

2.1 General features

- JEDEC (JC-42.4) SO-DIMM temperature sensor plus 256-byte serial EEPROM for Serial Presence Detect (SPD)
- Optimized for voltage range: 3.0 V to 3.6 V, but SPD can be read down to 1.7 V
- Shutdown current: 0.1 μA (typ.) and 3.0 μA (max.)
- 2-wire interface: I²C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus Alert Response Address and TIMEOUT (programmable)
- ESD protection exceeds 2500 V HBM per JESD22-A114, 250 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Available packages: TSSOP8 and HVSON8

2.2 Temperature sensor features

- 11-bit ADC Temperature-to-Digital converter with 0.125 °C resolution
- Operating current: 250 μA (typ.) and 400 μA (max.)
- Programmable hysteresis threshold: off, 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature $\overline{\text{EVENT}}$ output
- SE97PW/1, SE97TK/1 B-grade accuracy: ±0.5 °C/±1 °C (typ./max.) → –20 °C to +125 °C
- SE97PW, SE97TK C-grade accuracy: ±0.5 °C/±2 °C (typ./max.) → –20 °C to +125 °C

2.3 Serial EEPROM features

- Operating current:
  - Write → 0.6 mA (typ.) for 3.5 ms (typ.)
  - Read → 100 μA (typ.)
- Organized as 1 block of 256 bytes [(256 × 8) bits]
- 100,000 write/erase cycles and 10 years of data retention
- Permanent and Reversible Software Write Protect
- Software Write Protection for the lower 128 bytes

3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking

- Hard disk drives and other PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE97PW	SE97	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE97PW/1	97/1			
SE97TK	SE97	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1
SE97TK/1	97/1			

5. Block diagram

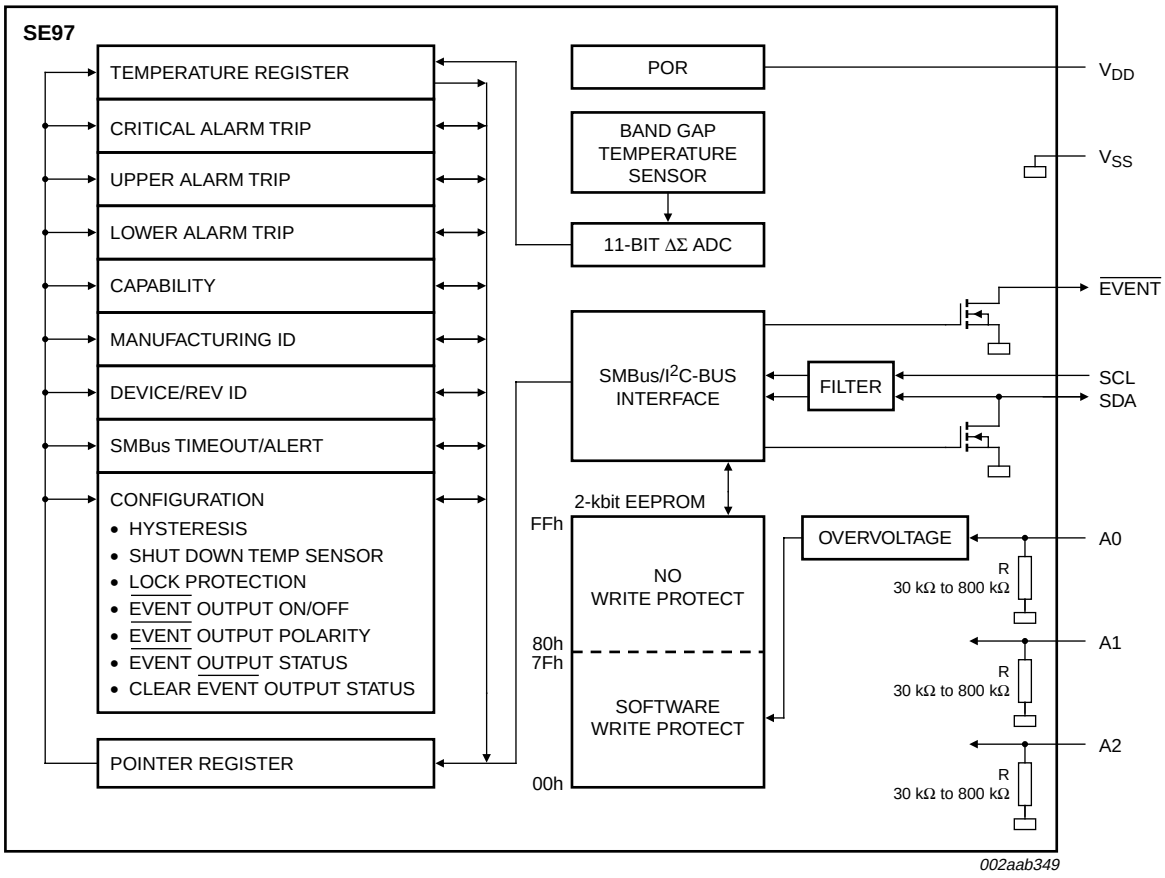


Fig 1. Block diagram of SE97

6. Pinning information

6.1 Pinning

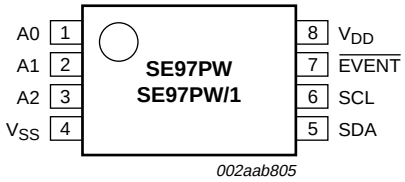


Fig 2. Pin configuration for TSSOP8

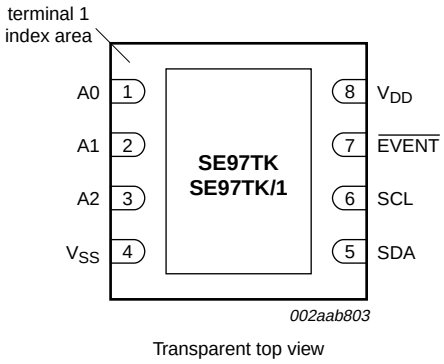


Fig 3. Pin configuration for HVSON8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	1	I	I^2C-bus/SMBus slave address bit 0 with internal pull-down. This input is overvoltage tolerant to support software write protection.
A1	2	I	I^2C-bus/SMBus slave address bit 1 with internal pull-down
A2	3	I	I^2C-bus/SMBus slave address bit 2 with internal pull-down
V_{SS}	4	ground	device ground
SDA	5	I/O	SMBus/I^2C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I^2C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
$\overline{EVENT}$	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V_{DD}	8	power	device power supply (3.0 V to 3.6 V); supports 1.7 V for EEPROM read only.

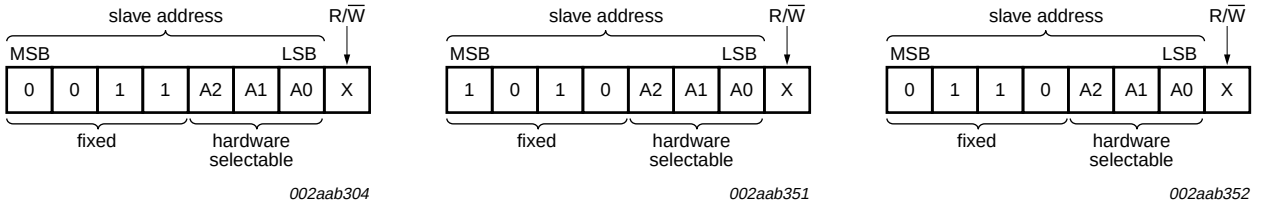
7. Functional description

7.1 Serial bus interface

The SE97 communicates with a host controller by means of the 2-wire serial bus (I^2C-bus/SMBus) that consists of a serial clock (SCL) and serial data (SDA) signals. The device supports SMBus, I^2C-bus Standard-mode and Fast-mode. The I^2C-bus standard speed is defined to have bus speeds from 0 Hz to 100 kHz, I^2C-bus fast speed from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE97 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one byte at a time with the Most Significant Bit (MSB) is transferred first. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

7.2 Slave address

The SE97 uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to co-exist on the same bus. The A0, A1 and A2 pins are pulled LOW internally. The A0 pin is also overvoltage tolerant supporting 10 V software write protect. When it is driven higher than 7 V, writing a special command would put the EEPROM in reversible write protect mode (see Section 7.10.2 “Memory Protection”). Each pin is sampled at the start of each I^2C-bus/SMBus access. The temperature sensor’s fixed address is ‘0011b’. The EEPROM’s fixed address for the normal EEPROM read/write is ‘1010b’, and for EEPROM software protection command is ‘0110b’. Refer to Figure 4.



a. Temperature sensor

b. EEPROM (normal read/write)

c. EEPROM (software protection command)

Fig 4. Slave address

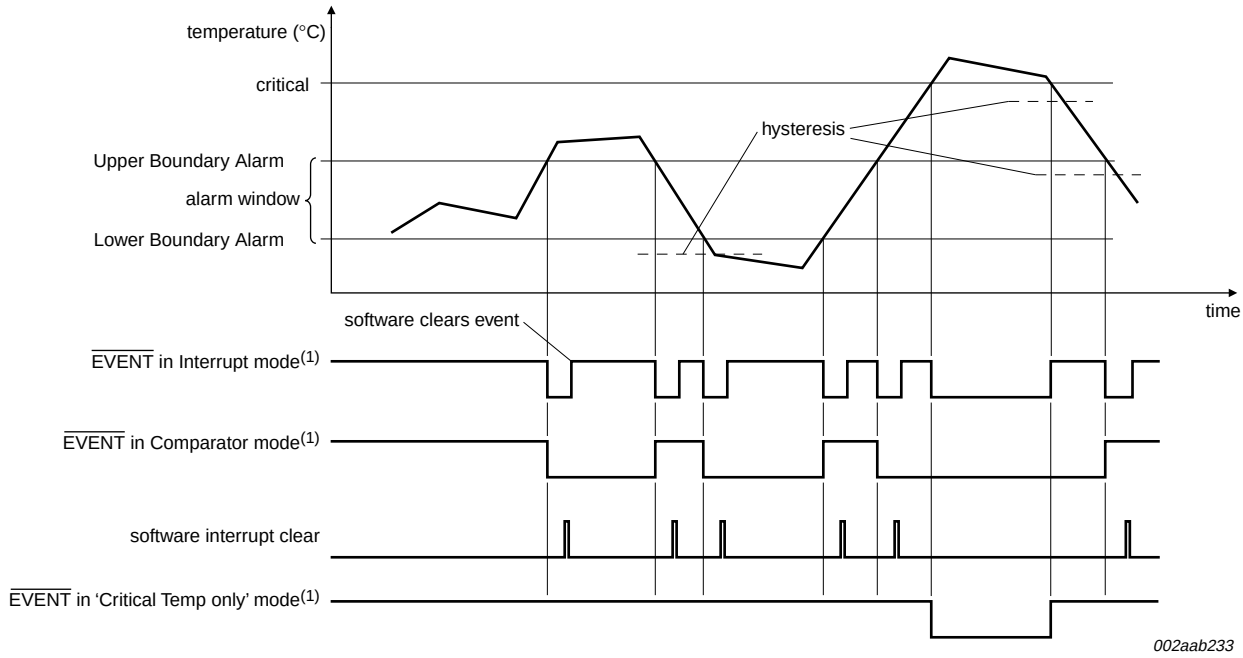
7.3 $\overline{\text{EVENT}}$ output

The $\overline{\text{EVENT}}$ pin is an open-drain output whose function can be programmed as an interrupt, comparator, or critical alarm mode. When the device operates in Interrupt mode, and the temperature reaches a critical temperature, the device switches to the comparator mode automatically and asserts the $\overline{\text{EVENT}}$ pin. When the temperature drops below critical temperature, the device reverts back to either interrupt or comparator mode, as programmed in the Configuration Register. The interrupt latch can be cleared by writing a ‘1’ to the ‘Clear $\overline{\text{EVENT}}$’ bit (CEVNT) in the Configuration Register or by performing the SMBus Alert Response Address (ARA).

The $\overline{\text{EVENT}}$ output is typically pulled up to a voltage level from 0.9 V to 3.6 V with an external pull-up resistor, but there is no real lower limit on the pull-up voltage for the $\overline{\text{EVENT}}$ pin since it is simply an open-drain output. It could be pulled up to 0.1 V and

would not affect the SE97. From the system perspective, there will be a practical limit. That limit will be the voltage necessary for the device monitoring in the interrupt pin to detect a HIGH on its input. A possible practical limit for a CMOS input would be 0.4 V. Another thing to consider is the value of the pull-up resistor. When a low supply voltage is applied to the drain (through the pull-up resistor) it is important to use a higher value pull-up resistor, to allow a larger maximum signal swing on the $\overline{\text{EVENT}}$ pin. An example would be if a 150 Ω resistor were used as the pull-up to 0.9 V, the output would only toggle between 0.9 V and 0.45 V, which may not be enough voltage swing to detect on the receiver end. As long as a reasonable pull-up resistor is used (> 1 kΩ) and the receiver has a low input switching threshold (less than the pull-up voltage), there should no problem.

In comparator mode, the $\overline{\text{EVENT}}$ pin remains asserted until the temperature falls below the value programmed in the Upper Boundary Alarm Trip Register or rises above the value programmed in the Lower Boundary Alarm Trip register, or until the range of these alarm registers are reprogrammed and the temperature falls inside the alarm limits. Figure 5 depicts the $\overline{\text{EVENT}}$ output for all the three modes. All event thresholds use hysteresis as programmed in the Configuration Register.



(1) $\overline{\text{EVENT}}$ pin shown here is active LOW. It can be programmed to be active HIGH.

Fig 5. $\overline{\text{EVENT}}$ output for 'Interrupt', 'Comparator', and 'Critical Temp only' modes

7.3.1 Alarm window

The alarm window consists of two registers: an Upper Boundary Alarm Trip register (02h), and a Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point. When the $\overline{\text{EVENT}}$ control is enabled, the $\overline{\text{EVENT}}$ output will be triggered whenever entering or exiting the alarm window.

7.3.2 Critical trip

The device can be programmed in such a way that the $\overline{\text{EVENT}}$ output is triggered when the temperature exceeds the critical trip point set by the Critical Alarm Trip register (04h).

When the temperature sensor reaches the critical temperature value, the device is automatically placed in comparator mode; the $\overline{\text{EVENT}}$ output is only cleared when the temperature falls below the critical temperature value and cannot be cleared through the clear $\overline{\text{EVENT}}$ bit or SMBus ALERT.

7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE97's conversion rate is at least 8 Hz or 125 ms.

7.5 Power-up default condition

After power-on, the SE97 is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared; $\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to '00h'
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to '0015h' for the C-grade and to '0017h' for the B-grade
- Operational mode: comparator
- SMBus register is defaulted to '00h'

7.6 Device initialization

SE97 temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain $\overline{\text{EVENT}}$ output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

Table 3 shows the default values and the example value to be programmed to these registers.

Table 3. Registers to be initialized

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register • hysteresis = 1.5 °C • $\overline{\text{EVENT}}$ output = Interrupt mode • $\overline{\text{EVENT}}$ output is enabled
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = –20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

7.7 SMBus TIMEOUT

The SE97 supports SMBus TIMEOUT feature. If the host holds SCL LOW more than 35 ms, the SE97 would reset its internal state machine to the bus IDLE state to prevent the system bus hang-up. This feature is turned on by default. The SMBus TIMEOUT is disabled by writing a '1' to bit 7 of register 22h.

Remark: When SMBus TIMEOUT is enabled, the I^2C-bus minimum bus speed is limited by the SMBus TIMEOUT specification limit of 10 kHz.

7.8 SMBus Alert Response Address (ARA)

The SE97 supports SMBus ALERT when it is programmed for the Interrupt mode and when the $\overline{\text{EVENT}}$ polarity bit is set to '0'. The $\overline{\text{EVENT}}$ pin can be ANDed with other $\overline{\text{EVENT}}$ or interrupt signals from other slave devices to signal their intention to communicate with the host controller. When the host detects $\overline{\text{EVENT}}$ or other interrupt signal LOW, it issues an ARA to which a slave device would respond with its address. When there are multiple slave devices generating an ALERT the SE97 performs bus arbitration with the other slaves. If it wins the bus, it responds to the ARA and then clears the $\overline{\text{EVENT}}$ pin.

Remark: Either in comparator mode or when the SE97 crosses the critical temperature, the host must also read the $\overline{\text{EVENT}}$ status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the $\overline{\text{EVENT}}$ pin will not get de-asserted.

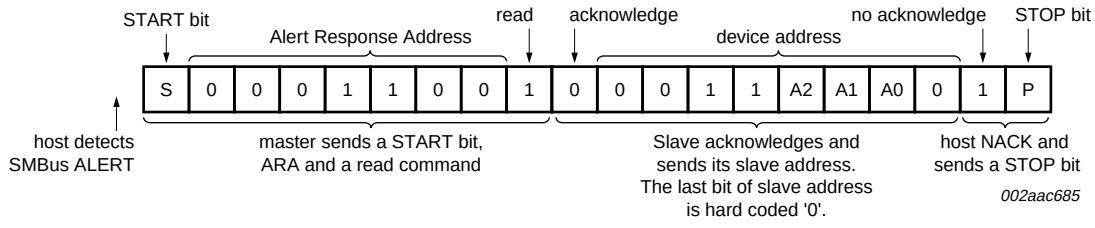


Fig 6. How SE97 responds to SMBus Alert Response Address

7.9 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer Register. At power-up, the Pointer Register is set to '00h', the location for the Capability Register. The Pointer Register latches the last location to which it was set. Each data register falls into one of three types of user accessibility:

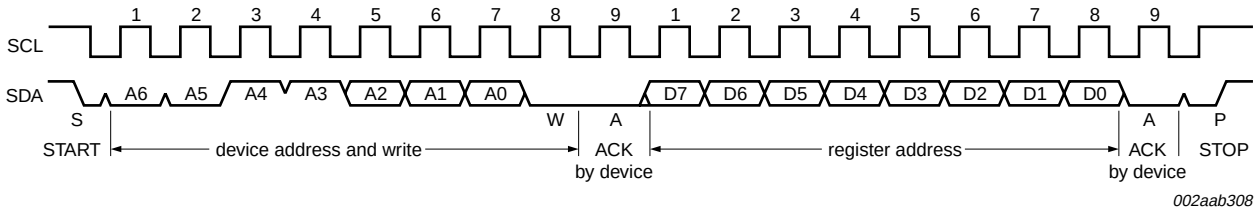
- Read only
- Write only
- Write/Read same address

A 'write' to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

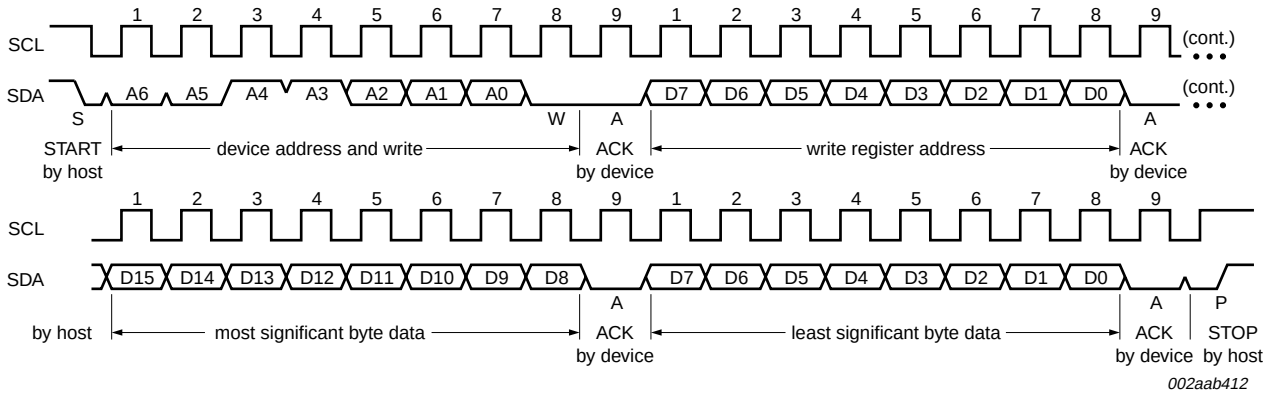
- If the location latched in the Pointer Register is correct (most of the time it is expected that the Pointer Register will point to one of the Temperature Register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer Register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to timing diagrams Figure 7 to Figure 10 for how to program the device.



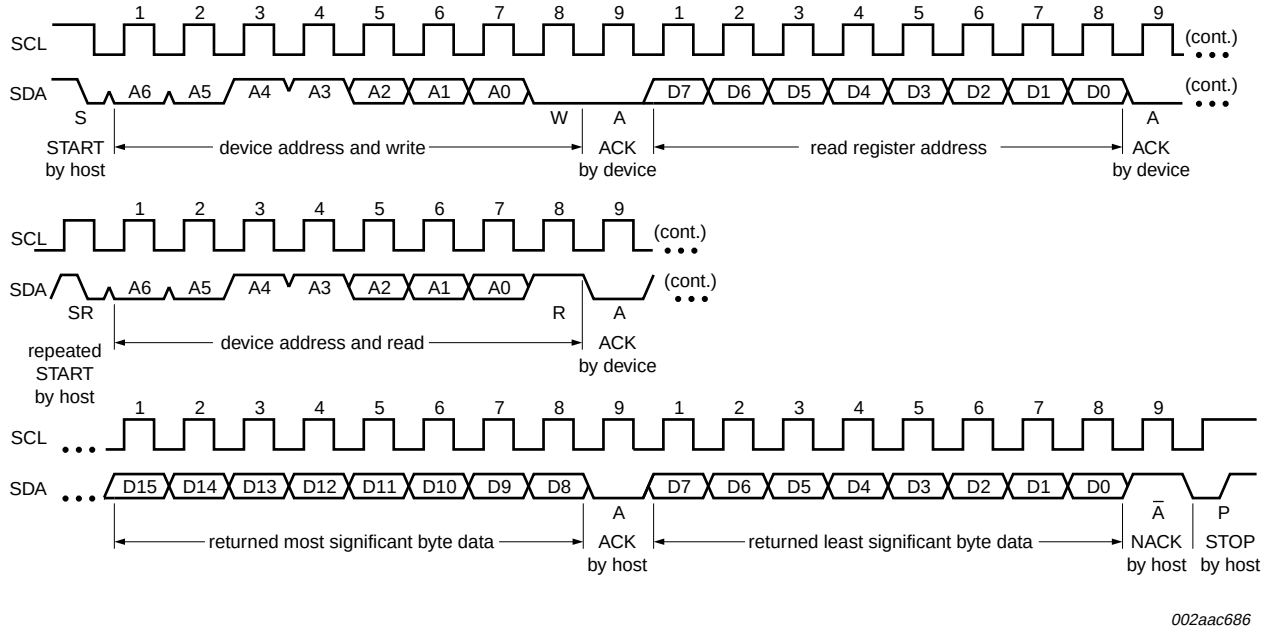
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 7. SMBus/I²C-bus write to the Pointer Register



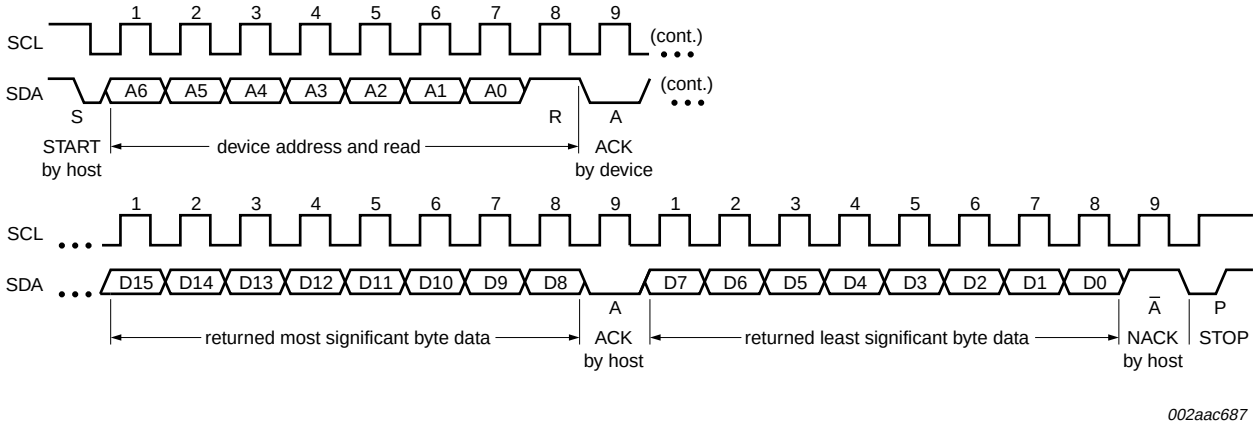
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 8. SMBus/I²C-bus write to the Pointer Register followed by a write data word



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 9. SMBus/I²C-bus write to Pointer Register followed by a repeated START and an immediate data word read



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 10. SMBus/I²C-bus word read from register with a pre-set pointer

7.10 EEPROM operation

The 2-kbit EEPROM is organized as either 256 bytes of 8 bits each (byte mode), or 16 pages of 16 bytes each (page mode). Accessing the EEPROM in byte mode or page mode is automatic; partial page write of 2 bytes, 4 bytes, or 8 bytes is also supported. Communication with the EEPROM is via the 2-wire serial I²C-bus or SMBus. Figure 11 provides an overview of the EEPROM partitioning.

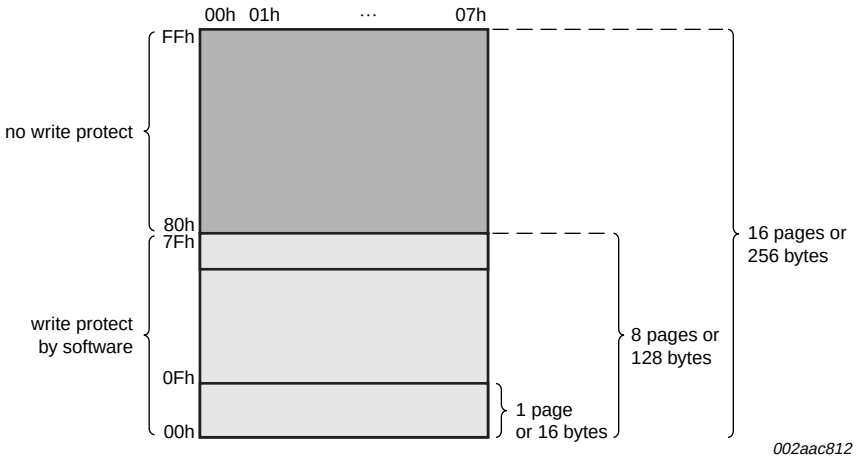


Fig 11. EEPROM partitioning

7.10.1 Write operations

7.10.1.1 Byte Write

In Byte Write mode the master creates a START condition and then broadcasts the slave address, byte address, and data to be written. The slave acknowledges all 3 bytes by pulling down the SDA line during the ninth clock cycle following each byte. The master creates a STOP condition after the last ACK from the slave, which then starts the internal write operation (see Figure 12). During internal write, the slave will ignore any read/write request from the master.

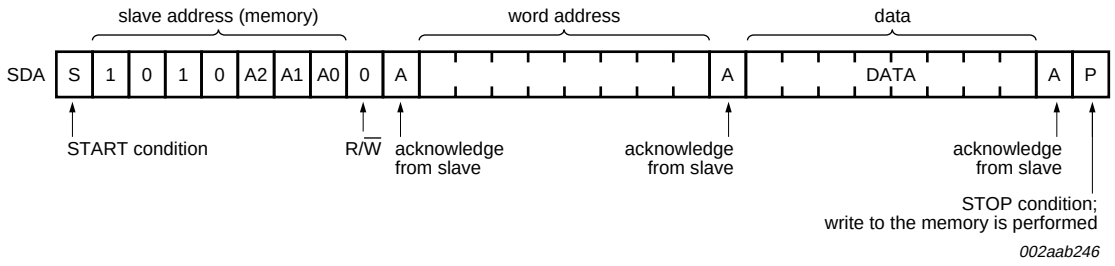


Fig 12. Byte Write timing

7.10.1.2 Page Write

The SE97 contains 256 bytes of data, arranged in 16 pages of 16 bytes each. The page is selected by the four Most Significant Bits (MSB) of the address byte presented to the device after the slave address, while the four Least Significant Bits (LSB) point to the byte within the page. By loading more than one data byte into the device, up to an entire page can be written in one write cycle (see Figure 13). The internal byte address counter will increment automatically after each data byte. If the master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a wrap-around fashion within the selected page. The internal write cycle is started following the STOP condition created by the master.

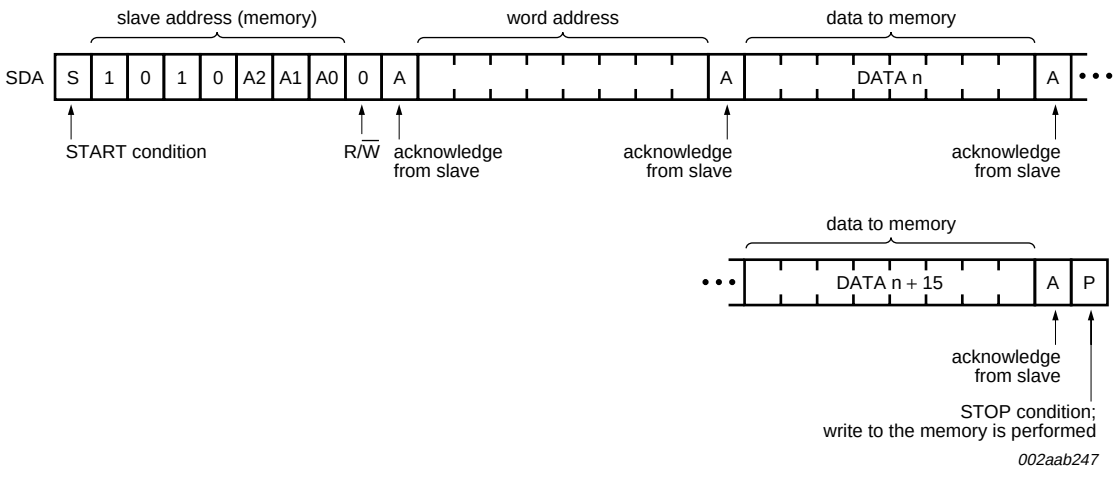


Fig 13. Page Write timing

7.10.1.3 Acknowledge polling

Acknowledge polling can be used to determine if the SE97 is busy writing or is ready to accept commands. Polling is implemented by sending a 'Selective Read' command (described in Section 7.10.3 "Read operations") to the device. The SE97 will not acknowledge the slave address as long as internal write is in progress.

7.10.2 Memory Protection

The lower half (the first 128 bytes) of the memory can be write protected by special EEPROM commands without an external control pin. The SE97 features three types of memory write protection instructions, and three respective read Protection instructions. The level of write-protection (set or clear) that has been defined using these instructions remained defined even after power cycle.

The memory protection commands are:

- Permanent Write Protection (PWP)
- Reversible Write Protection (RWP)
- Clear Write Protection (CWP)
- Read Permanent Write Protection (RPWP)
- Read Reversible Write Protection (RRWP)
- Read Clear Write Protection (RCWP)

Table 4 is the summary for normal and memory protection instructions.

Table 4. EEPROM commands summary

Command	Fixed address				Hardware selectable address			R/$\overline{W}$
	Bit 7[1]	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal EEPROM read/write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Reversible Write Protection (RWP)	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	0
Clear Reversible Write Protection (CRWP)	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	0
Permanent Write Protection (PWP)[2]	0	1	1	0	A2	A1	A0	0
Read RWP	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	1
Read CRWP	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	1
Read PWP	0	1	1	0	A2	A1	A0	1

[1] The most significant bit, bit 7, is sent first.

[2] A0, A1, and A2 are compared against the respective external pins on the SE97.

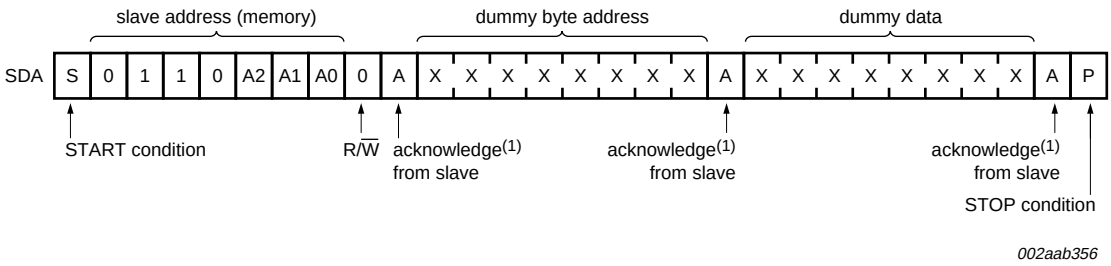
[3] $V_{I(ov)}$ ranges from 7 V to 10 V.

This special EEPROM command consists of a unique 4-bit fixed address (0110b) and the voltage level applied on the 3-bit hardware address. Normally, to address the memory array, the 4-bit fixed address is '1010b'. To access the memory protection settings, the 4-bit fixed address is '0110b'. Figure 14 and Figure 15 show the write and read protection sequence, respectively.

Up to eight memory devices can be connected on a single I²C-bus. Each one is given a 3-bit on the hardware selectable address (A2, A1, A0) inputs. The device only responds when the 4-bit fixed and hardware selectable bits are matched. The 8th bit is the read/write bit. This bit is set to 1 or 0 for read and write protection, respectively.

The corresponding device acknowledges during the ninth bit time when there is a match on the 7-bit address.

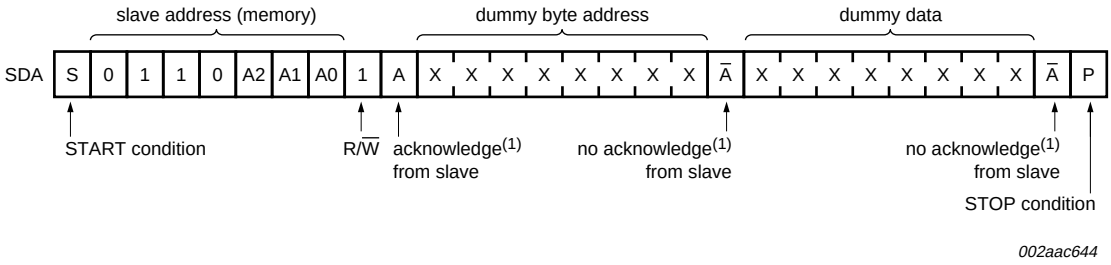
The device does not acknowledge when there is no match on the 7-bit address or when the device is already in permanent write protection mode and is programmed with any write protection instructions (i.e., PWP, RWP, CWP).



X = Don't Care

(1) Refer to Table 5 regarding the exact state of the acknowledge bit.

Fig 14. Software Write Protect (write)



X = Don't Care

(1) Refer to Table 6 regarding the exact state of the acknowledge bit.

Fig 15. Software Write Protect (read)

7.10.2.1 Permanent Write Protection (PWP)

If the software write-protection has been set with the PWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PWP instruction has been successfully executed, the device no longer acknowledges any instruction (with 4-bit fixed address of 0110b) to access the write-protection settings.

7.10.2.2 Reversible Write Protection (RWP) and Clear Reversible Write Protection (CRWP)

If the software write-protection has been set with the RWP instruction, it can be cleared again with a CRWP instruction.

The two instructions, RWP and CRWP have the same format as a Byte Write instruction, but with a different setting for the hardware address pins (as shown in Table 4). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all 'Don't Care' (Figure 14). Another difference is that the voltage, $V_{I(ov)}$, must be applied on the A0 pin, and specific logical levels must be applied on the other two (A1 and A2), as shown in Table 4.

Table 5. Acknowledge when writing data or defining write protection

Instructions with R/$\overline{W}$ bit = 0.

Status	Instruction	ACK	Address	ACK	Data byte	ACK	Write cycle ($T_{cy(W)}$)
Permanently protected	PWP, RWP or CRWP	NACK	not significant	NACK	not significant	NACK	no
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Protected with RWP	RWP	NACK	not significant	NACK	not significant	NACK	no
	CRWP	ACK	not significant	ACK	not significant	ACK	yes
	PWP	ACK	not significant	ACK	not significant	ACK	yes
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Not protected	PWP or RWP	ACK	not significant	ACK	not significant	ACK	yes
	CRWP	ACK	not significant	ACK	not significant	ACK	no
	page or byte write	ACK	address	ACK	data	ACK	yes

7.10.2.3 Read Permanent Write Protection (RPWP), Read Reversible Write Protection (RRWP), and Read Clear Reversible Write Protection (RCRWP)

Read PWP, RWP, and CRWP allow the SE97 to be read in write protection mode. The instruction format is the same as that of the write protection except that the 8th bit, R/$\overline{W}$, is set to 1. Figure 15 shows the instruction format, while Table 6 shows the responses when the instructions are issued.

Table 6. Acknowledge when reading the write protection

Instructions with R/$\overline{W}$ bit = 1.

Status	Instruction	ACK	Address	ACK	Data byte	ACK
Permanently protected	RPWP, RRWP or RCRWP	NACK	not significant	NACK	not significant	NACK
Protected with RWP	RRWP	NACK	not significant	NACK	not significant	NACK
	RCRWP	ACK	not significant	NACK	not significant	NACK
	RPWP	ACK	not significant	NACK	not significant	NACK
Not protected	RPWP, RRWP or RCRWP	ACK	not significant	NACK	not significant	NACK

7.10.3 Read operations

7.10.3.1 Current address read

In Standby mode, the SE97 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If the ‘previous’ byte was the last byte in memory, then the address counter will point to the first memory byte, and so on. If the SE97 decodes a slave address with a ‘1’ in the R/$\overline{W}$ bit position (Figure 16), it will issue an Acknowledge in the ninth clock cycle and will then transmit the data byte being pointed at by the address counter. The master can then stop further transmission by issuing a No Acknowledge on the ninth bit then followed by a STOP condition.

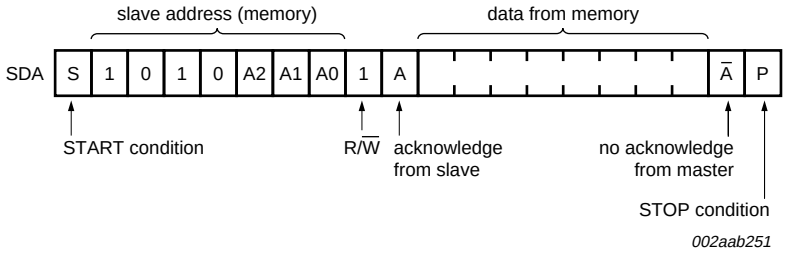


Fig 16. Current address read timing

7.10.3.2 Selective read

The read operation can also be started at an address different from the one stored in the address counter. The address counter can be ‘initialized’ by performing a ‘dummy’ write operation (Figure 17). The START condition is followed by the slave address (with the R/$\overline{W}$ bit set to ‘0’) and the desired byte address. Instead of following-up with data, the master then issues a second START, followed by the ‘Current Address Read’ sequence, as described in Section 7.10.3.1.

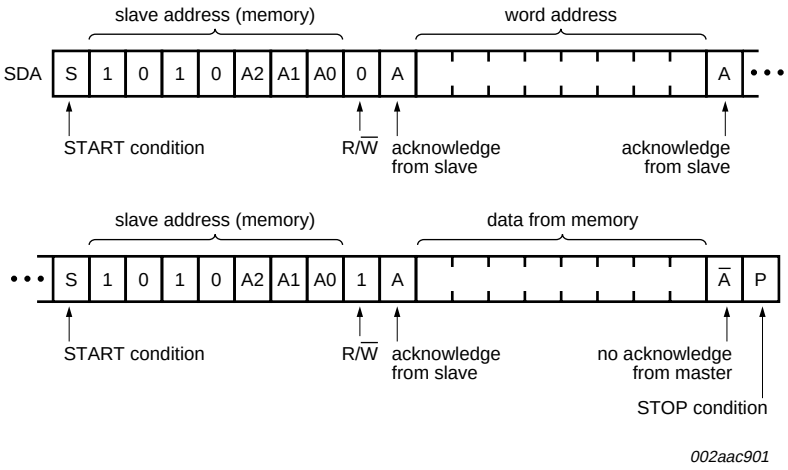


Fig 17. Selective read timing

7.10.3.3 Sequential read

If the master acknowledges the first data byte transmitted by the SE97, then the device will continue transmitting as long as each data byte is acknowledged by the master (Figure 18). If the end of memory is reached during sequential Read, the address counter will 'wrap around' to the beginning of memory, and so on. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

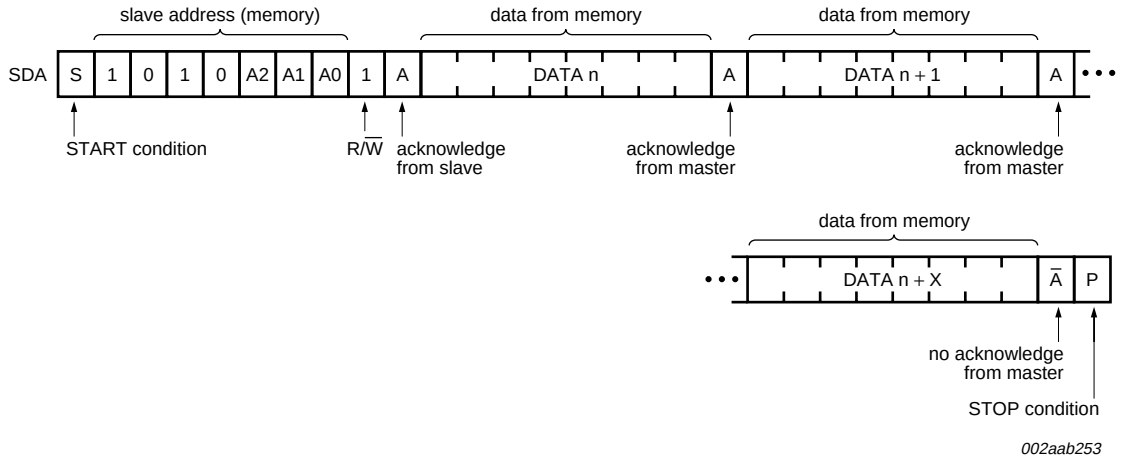


Fig 18. Sequential read timing

8. Register descriptions

8.1 Register overview

This section describes all the registers used in the SE97. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading '0's. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

Table 7. Register summary

Address (hex)	Default state (hex)	Register name
n/a	n/a	Pointer Register
00h	0015h/0017h	Capability Register (B-grade = 0017h, C-grade = 0015h)
01h	0000h	Configuration Register
02h	0000h	Upper Boundary Alarm Trip Register
03h	0000h	Lower Boundary Alarm Trip Register
04h	0000h	Critical Alarm Trip Register
05h	n/a	Temperature Register
06h	1131h	Manufacturer ID Register
07h	A200h	Device ID/Revision Register
08h to 21h	0000h	reserved registers
22h	0000h	SMBus Register
23h to FFh	0000h	reserved registers

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

8.2 Capability Register (00h, 16-bit read-only)

Table 8. Capability Register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RFU			TRES		WRNG	HACC	BCAP
Default	0	0	0	1	0	1	[1]	1
Access	R	R	R	R	R	R	R	R

[1] SE97PW, SE97TK = 1; SE97PW/1, SE97TK/1 = 0.

Table 9. Capability Register (address 00h) bit description

Bit	Symbol	Description
15:5	RFU	Reserved for future use; must be zero.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy bit set during manufacture. 0 — accuracy ±2 °C over the active range and ±3 °C over the monitor range (C-grade) 1 — high accuracy ±1 °C over the active range and ±2 °C over the monitor range (B-grade)
0	BCAP	Basic capability. 1 — has Alarm and Critical Trips capability

8.3 Configuration Register (01h, 16-bit read/write)

Table 10. Configuration Register (address 01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HEN		SHMD
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 11. Configuration Register (address 01h) bit description

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be ‘0’.
10:9	HEN	Hysteresis Enable. 00 — disable hysteresis (default) 01 — enable hysteresis at 1.5 °C 10 — enable hysteresis at 3 °C 11 — enable hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to ‘1’ (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary Register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 5 and Table 12). Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to ‘0’ (temperature is equal to or above the Alarm Window Lower Boundary Trip Register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary Register. As the temperature decreases, bit 13 will be set to ‘1’ when the value in the Temperature Register is equal to or less than the value in the Alarm Temperature Lower Boundary Register minus 3 °C. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits cannot be altered.
8	SHMD	Shutdown Mode. 0 — enabled Temperature Sensor (default) 1 — disabled Temperature Sensor When shut down, the thermal sensor diode and ADC are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time.

Table 11. Configuration Register (address 01h) bit description *…continued*

Bit	Symbol	Description
7	CTLB	Critical Trip Lock bit. 0 — Critical Alarm Trip Register is not locked and can be altered (default) 1 — Critical Alarm Trip Register settings cannot be altered This bit is initially cleared. When set, this bit will return a '1', and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes.
6	AWLB	Alarm Window Lock bit. 0 — Upper and Lower Alarm Trip Registers are not locked and can be altered (default) 1 — Upper and Lower Alarm Trip Registers setting cannot be altered This bit is initially cleared. When set, this bit will return a '1' and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes.
5	CEVNT	Clear $\overline{\text{EVENT}}$ (write only). 0 — no effect (default) 1 — clears active $\overline{\text{EVENT}}$ in Interrupt mode. Writing to this register has no effect in Comparator mode. When read, this register always returns zero.
4	ESTAT	$\overline{\text{EVENT}}$ Status (read only). 0 — $\overline{\text{EVENT}}$ output condition is not being asserted by this device (default) 1 — $\overline{\text{EVENT}}$ output pin is being asserted by this device due to Alarm Window or Critical Trip condition The actual event causing the event can be determined from the Read Temperature Register. Interrupt Events can be cleared by writing to the 'Clear $\overline{\text{EVENT}}$' bit (CEVNT). Writing to this bit will have no effect.
3	EOCTL	$\overline{\text{EVENT}}$ Output Control. 0 — $\overline{\text{EVENT}}$ output disabled (default) 1 — $\overline{\text{EVENT}}$ output enabled When either of the lock bits is set, this bit cannot be altered until unlocked.
2	CVO	Critical Event Only. 0 — $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (default) 1 — $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register When the alarm window lock bit is set, this bit cannot be altered until unlocked.
1	EP	$\overline{\text{EVENT}}$ Polarity. 0 — active LOW (default) 1 — active HIGH. When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked.
0	EMD	$\overline{\text{EVENT}}$ Mode. 0 — comparator output mode (default) 1 — interrupt mode When either of the alarm or critical lock bits is set, this bit cannot be altered until unlocked.

Table 12. Hysteresis Enable

Action	Below Alarm Window bit (bit 13)		Above Alarm Window bit (bit 14)		Above Critical Trip bit (bit 15)	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
sets	falling	lower alarm threshold – hysteresis	rising	upper alarm threshold	rising	critical alarm threshold
clears	rising	lower alarm threshold	falling	upper alarm threshold – hysteresis	falling	critical alarm threshold – hysteresis

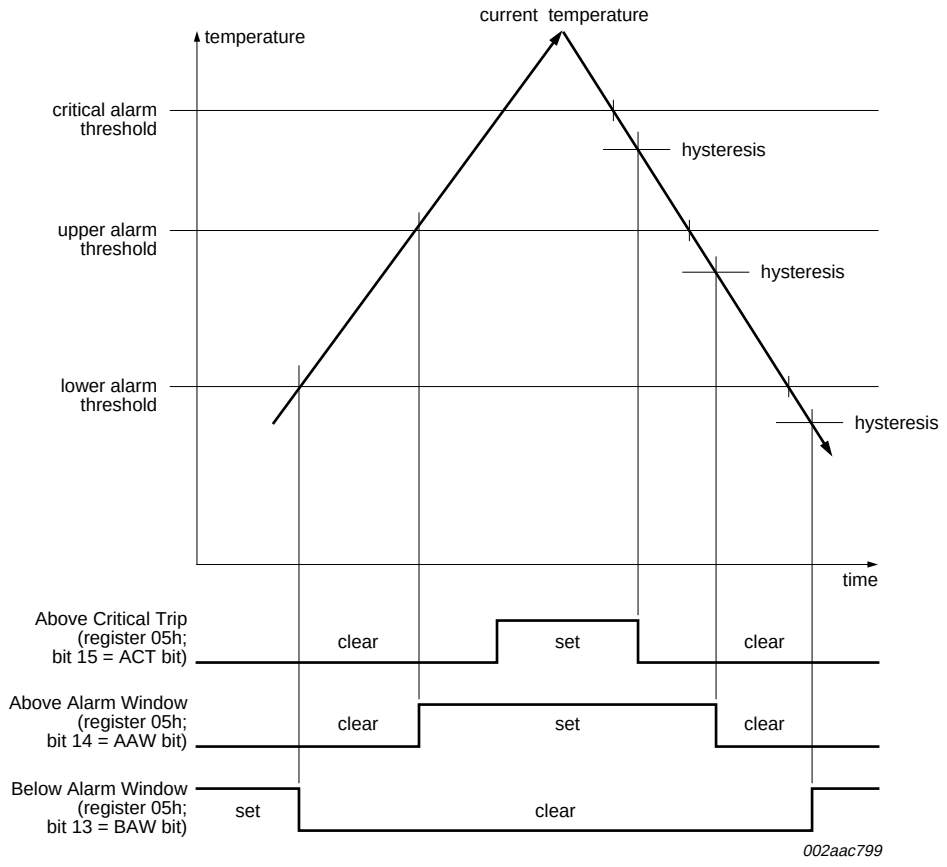


Fig 19. Hysteresis: how it works

8.4 Temperature format

The temperature data from the temperature read back register is an 11-bit 2's complement word with the least significant bit (LSB) equal to 0.125 °C (resolution).

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent −25.75 °C.

The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the $\overline{\text{EVENT}}$ output.

Table 13 lists the examples of the content of the temperature data register for positive and negative temperature for two scenarios of status bits: status bits = 000b and status bits = 111b.

Table 13. Degree Celsius and Temperature Data register

Temperature	Content of Temperature Data register			
	Status bits = 000b		Status bits = 111b	
	Binary	Hex	Binary	Hex
+125 °C	000 0 01111101 000 0	07D0h	111 0 01111101 000 0	E7D0h
+25 °C	000 0 00011001 000 0	0190h	111 0 00011001 000 0	E190h
+1 °C	000 0 00000001 000 0	0010h	111 0 00000001 000 0	E010h
+0.25 °C	000 0 00000000 010 0	0004h	111 0 00000000 010 0	E004h
+0.125 °C	000 0 00000000 001 0	0002h	111 0 00000000 001 0	E002h
0 °C	000 0 00000000 000 0	0000h	111 0 00000000 000 0	E000h
−0.125 °C	000 1 11111111 111 0	1FFEh	111 1 11111111 111 0	FFFEh
−0.25 °C	000 1 11111111 110 0	1FFCh	111 1 11111111 110 0	FFFCh
−1 °C	000 1 11111111 000 0	1FF0h	111 1 11111111 000 0	FFF0h
−20 °C	000 1 11110100 000 0	1F40h	111 1 11110100 000 0	FF40h
−25 °C	000 1 11100111 000 0	1E70h	111 1 11100111 000 0	FE70h
−55 °C	000 1 11001001 000 0	1C90h	111 1 11001001 000 0	FC90h

8.5 Temperature Trip Point registers

8.5.1 Upper Boundary Alarm Trip Register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 14. Upper Boundary Alarm Trip Register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	UBT			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	UBT						RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 15. Upper Boundary Alarm Trip Register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	UBT	Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.5.2 Lower Boundary Alarm Trip Register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 16. Lower Boundary Alarm Trip Register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol		RFU		SIGN		LBT		
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol				LBT			RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 17. Lower Boundary Alarm Trip Register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	LBT	Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.5.3 Critical Alarm Trip Register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

Table 18. Lower Boundary Alarm Trip Register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol		RFU		SIGN		CT		
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol				CT			RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 19. Critical Alarm Trip Register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	CT	Critical Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.6 Temperature Register (16-bit read-only)

Table 20. Temperature Register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ACT	AAW	BAW	SIGN	TEMP			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TEMP							RFU
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 21. Temperature Register bit description

Bit	Symbol	Description
15	ACT	Above Critical Trip. 0 — temperature is below the Critical Alarm Trip Register setting 1 — temperature is equal to or above the Critical Alarm Trip Register setting
14	AAW	Above Alarm Window. 0 — temperature is equal to or below the Upper Boundary Alarm Trip Register 1 — temperature is above the Alarm window
13	BAW	Below Alarm Window. 0 — temperature is equal to or above the Lower Boundary Alarm Trip Register 1 — temperature is below the Alarm window
12	SIGN	Sign bit. 0 — positive temperature value 1 — negative temperature value
11:1	TEMP	Temperature Value (2's complement). (LSB = 0.125 °C)
0	RFU	reserved; always '0'

8.7 Manufacturer's ID register (16-bit read-only)

The SE97 Manufacturer's ID register is intended to match Philips PCI-SIG (1131h).

Table 22. Manufacturer's ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Default	0	0	0	1	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	(cont.)							
Default	0	0	1	1	0	0	0	1
Access	R	R	R	R	R	R	R	R

8.8 Device ID register

The SE97 device ID and device revision are A1h and 00h, respectively.

Table 23. Device ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Default	1	0	1	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Device revision							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

8.9 SMBus register

Table 24. SMBus Timeout register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	STMOUT	RFU						SALRT
Default	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R/W

Table 25. SMBus Timeout register bit description

Bit	Symbol	Description
15:8	RFU	reserved; always ‘0’
7	STMOUT	SMBus time-out. 0 — SMBus time-out is enabled (default) 1 — disable SMBus time-out When either of the lock bits is set, this bit cannot be altered until unlocked.
6:1	RFU	reserved; always ‘0’
0	SALRT	SMBus Alert Response Address (ARA). 0 — SMBus ARA is enabled (default) 1 — disable SMBus ARA When either of the lock bits is set, this bit cannot be altered until unlocked.

9. Application design-in information

In a typical application, the SE97 behaves as a slave device and interfaces to a bus master (or host) via the SCL and SDA lines. The $\overline{\text{EVENT}}$ output is monitored by the host, and asserts when the temperature reading exceeds the programmed values in the alarm registers. The A0, A1 and A2 pins are directly connected to V_{DD} or V_{SS} without any pull-up resistors. The SDA and SCL serial interface pins are open-drain I/Os that require pull-up resistors, and are able to sink a maximum of 3 mA with a voltage drop less than 0.4 V. Typical pull-up values for SCL and SDA are 10 kΩ, but the resistor values can be changed in order to meet the rise time requirement if the capacitance load is too large due to routing, connectors, or multiple components sharing the same bus.

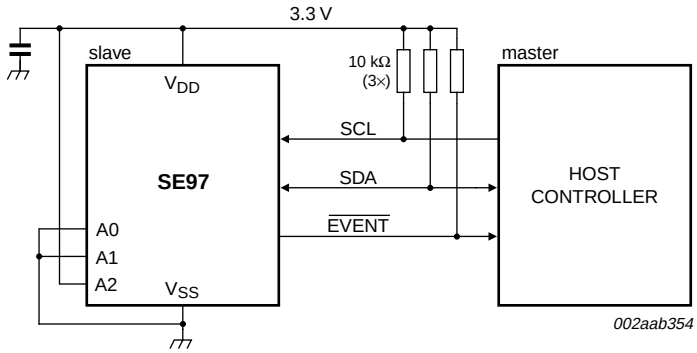


Fig 20. Typical application showing SE97 interfacing with 3.3 V host

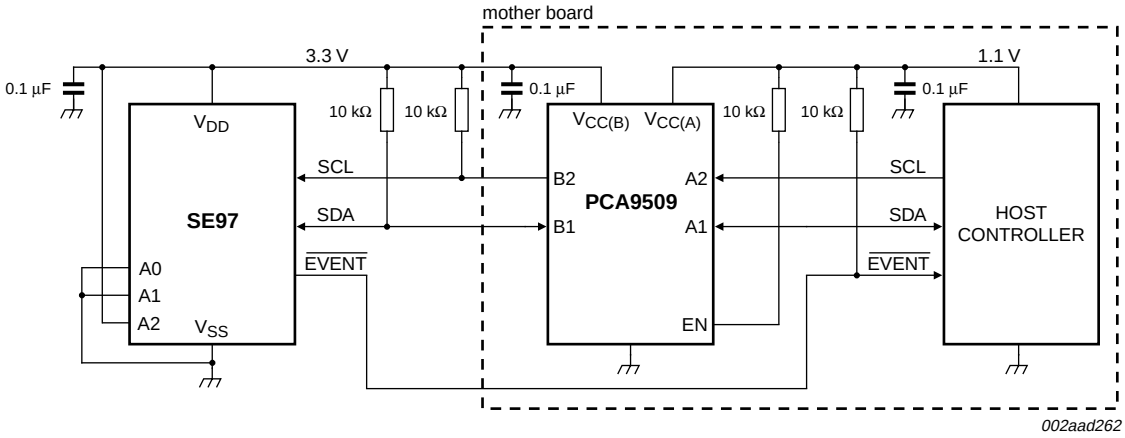


Fig 21. SE97 interfacing with 1.1 V host controller

9.1 SE97 in memory module application

Figure 22 shows the SE97 being placed in the memory module application. The SE97 is centered in the memory module to monitor the temperature of the DRAM and also to provide a 2-kbit EEPROM as the Serial Presence Detect (SPD). In the event of overheating, the SE97 triggers the $\overline{\text{EVENT}}$ output and the memory controller throttles the memory bus to slow the DRAM. The memory controller can also read the SE97 and watch the DRAM thermal behavior, taking preventive measures when necessary.

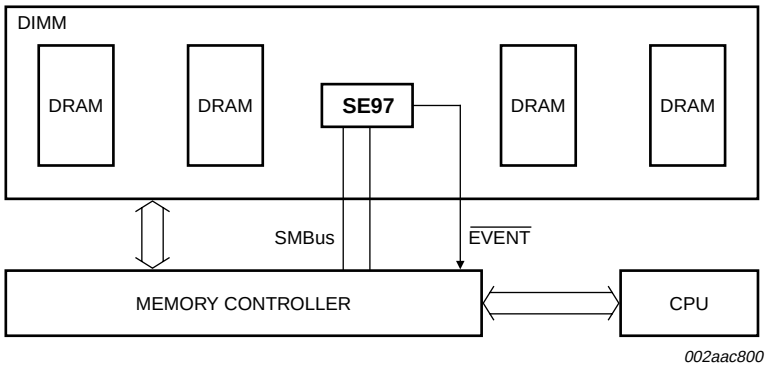


Fig 22. System application

9.2 Layout consideration

The SE97 does not require any additional components other than the host controller to read its temperature. It is recommended that a 0.1 µF bypass capacitor between the V_{DD} and V_{SS} pins is located as close as possible to the power and ground pins for noise protection.

9.3 Thermal considerations

In general, self-heating is the result of power consumption and not a concern, especially with the SE97, which consumes very low power. In the event the SDA and $\overline{\text{EVENT}}$ pins are heavily loaded with small pull-up resistor values, self-heating affects temperature accuracy by approximately 0.5 °C.

Equation 1 is the formula to calculate the effect of self-heating:

$$\Delta T = R_{th(j\text{-}a)} \times [(V_{DD} \times I_{DD(AV)}) + (V_{OL(SDA)} \times I_{OL(sink)(SDA)}) + (V_{OL(EVENT)} \times I_{OL(sink)EVENT})] \quad (1)$$

where:

$\Delta T = T_j - T_{amb}$

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = package thermal resistance

V_{DD} = supply voltage

$I_{DD(AV)}$ = average supply current

$V_{OL(SDA)}$ = LOW-level output voltage on pin SDA

$V_{OL(EVENT)}$ = LOW-level output voltage on pin $\overline{EVENT}$

$I_{OL(sink)(SDA)}$ = SDA output current LOW

$I_{OL(sink)EVENT}$ = $\overline{EVENT}$ output current LOW

Calculation example:

T_{amb} (typical temperature inside the notebook) = 50 °C

$I_{DD(AV)}$ = 400 µA

V_{DD} = 3.6 V

Maximum $V_{OL(SDA)}$ = 0.4 V

$I_{OL(sink)(SDA)}$ = 1 mA

$V_{OL(EVENT)}$ = 0.4 V

$I_{OL(sink)EVENT}$ = 3 mA

$R_{th(j-a)}$ of HVSON8 = 56 °C/W

$R_{th(j-a)}$ of TSSOP8 = 160 °C/W

Self heating due to power dissipation for HVSON8 is:

$$\Delta T = 56 \times [(3.6 \times 0.4) + (0.4 \times 3) + (0.4 \times 1)] = 56\ °C/W \times 3.04\ mW = 0.17\ °C \quad (2)$$

Self heating due to power dissipation for TSSOP8 is:

$$\Delta T = 160 \times [(3.6 \times 0.4) + (0.4 \times 3) + (0.4 \times 1)] = 160\ °C/W \times 3.04\ mV = 0.49\ °C \quad (3)$$

10. Limiting values

Table 26. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.2	V
V_n	voltage on any other pin	SDA, SCL, $\overline{EVENT}$ pins	–0.3	+4.2	V
V_{A0}	voltage on pin A0	overvoltage input; A0 pin	–0.3	12.5	V
I_{sink}	sink current	at SDA, SCL, $\overline{EVENT}$ pins	–1	50.0	mA
$T_{j(max)}$	maximum junction temperature		-	150	°C
T_{stg}	storage temperature		–65	+165	°C

11. Characteristics

Table 27. Characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −20 °C to +125 °C; unless otherwise specified.

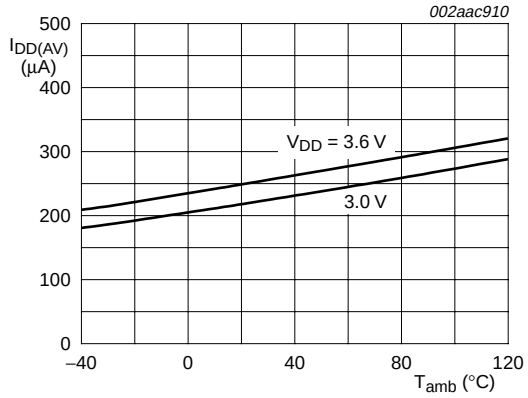
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{lim(acc)}$	temperature limit accuracy	B-grade; V_{DD} = 3.3 V ± 10 %				
		T_{amb} = −20 °C to +125 °C	−1.0	< ±0.5	+1.0	°C
		C-grade; V_{DD} = 3.3 V ± 10 %				
		T_{amb} = −20 °C to +125 °C	−2.0	< ±1	+2.0	°C
T_{res}	temperature resolution		-	0.25	-	°C
T_{conv}	conversion period	conversion time from STOP bit to conversion complete	-	100	120	ms
$E_{f(conv)}$	conversion rate error	percentage error in programmed data	−30	-	30	%

Table 28. DC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −20 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design.

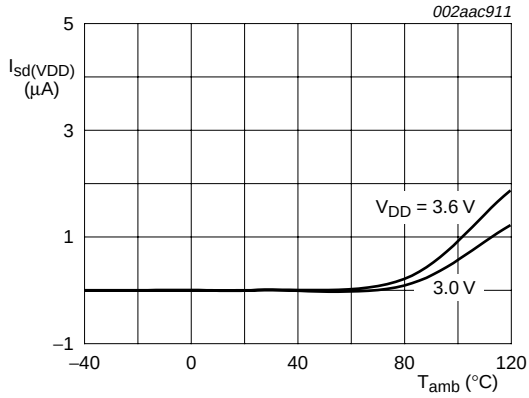
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(AV)}$	average supply current	SMBus inactive					
		V_{DD} = 3.0 V to 3.6 V		-	250	400	µA
		V_{DD} = 1.7 V		-	0.1	5.0	µA
$I_{sd(VDD)}$	supply voltage shutdown mode current	SMBus inactive		-	0.1	3	µA
V_{IH}	HIGH-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V		0.7 × V_{DD}	-	V_{DD} + 1	V
V_{IL}	LOW-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V		-	-	0.3 × V_{DD}	V
V_{OL1}	LOW-level output voltage 1	V_{DD} = 3.0 V; I_{OL} = 3 mA		-	-	0.4	V
V_{OL2}	LOW-level output voltage 2	V_{DD} = 1.7 V; I_{OL} = 1.5 mA		-	-	0.5	V
$V_{I(ov)}$	overvoltage input voltage	pin A0; $V_{I(ov)} - V_{DD}$ > 4.8 V	[1]	7	-	10	V
$I_{OL(sink)EVENT}$	LOW-level output sink current on pin $\overline{EVENT}$	V_{OL1} = 0.4 V		2	-	-	mA
$I_{OL(sink)(SDA)}$	LOW-level output sink current on pin SDA	V_{OL2} = 0.5 V		3	-	-	mA
I_{LOH}	HIGH-level output leakage current	$\overline{EVENT}$; $V_{OH} = V_{DD}$		−1.0	-	+1.0	µA
I_{LIH}	HIGH-level input leakage current	SDA, SCL; $V_I = V_{DD}$		−1.0	-	+1.0	µA
I_{LIL}	LOW-level input leakage current	SDA, SCL; $V_I = V_{SS}$		−1.0	-	+1.0	µA
		A0, A1, A2; $V_I = V_{SS}$		−1.0	-	+1.0	µA
$C_{i(SCL/SDA)}$	SCL and SDA input capacitance			-	5	10	pF
I_L	leakage current	on A0, A1, A2		-	1	-	µA
I_{pd}	pull-down current	internal; A0, A1, A2 pins; V_I = 0.3V_{DD} to V_{DD}		-	-	4.0	µA
Z_{IL}	LOW-level input impedance	pins A0, A1, A2; V_I < 0.3V_{DD}		30	-	-	kΩ
Z_{IH}	HIGH-level input impedance	pins A0, A1, A2		800	-	-	kΩ

[1] High-voltage input voltage applied to pin A0 during RWP and CRWP operations.



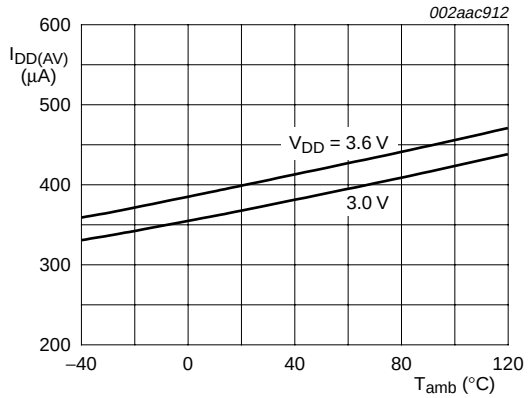
I^2C-bus and EEPROM inactive.

Fig 23. Average supply current



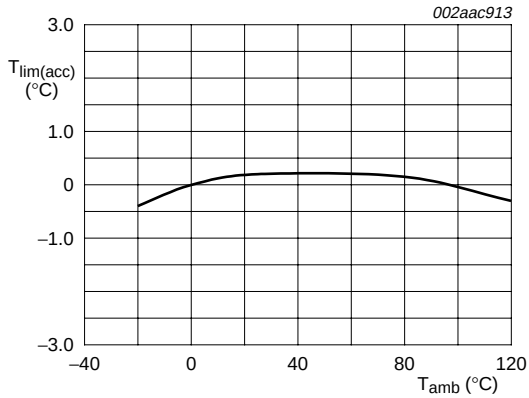
I^2C-bus, temp sensor and EEPROM inactive.

Fig 24. Shutdown supply current



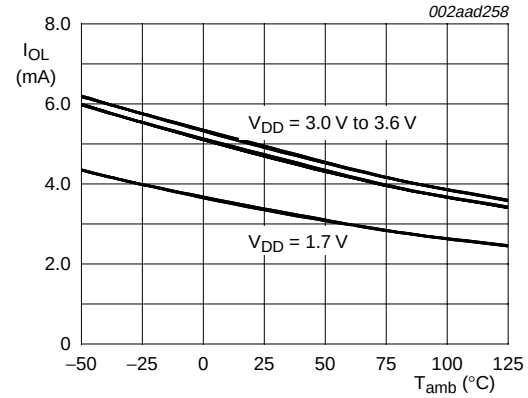
Temp sensor and EEPROM active.

Fig 25. Average supply current during EEPROM write



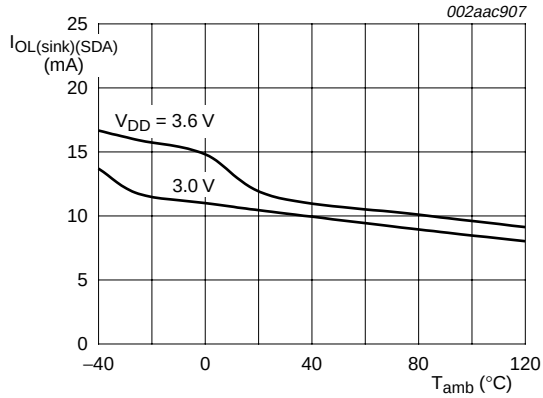
V_{DD} = 3.0 V to 3.6 V.

Fig 26. Typical temperature accuracy



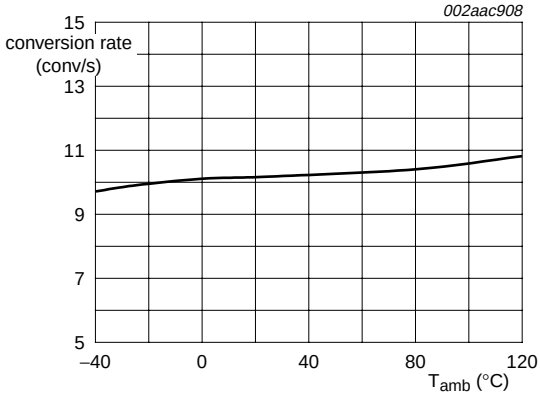
V_{OL} = 0.4 V.

Fig 27. $\overline{EVENT}$ output current



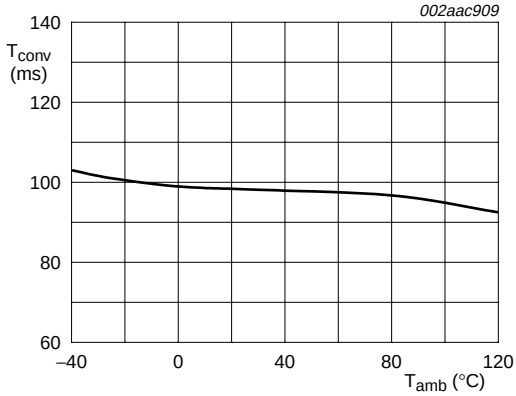
V_{OL} = 0.6 V.

Fig 28. SDA output current



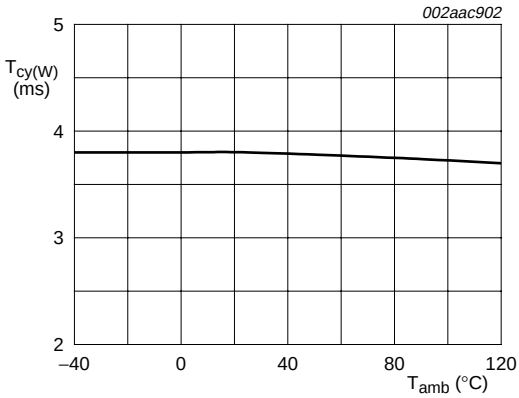
V_{DD} = 3.0 V to 3.6 V.

Fig 29. Conversion rate



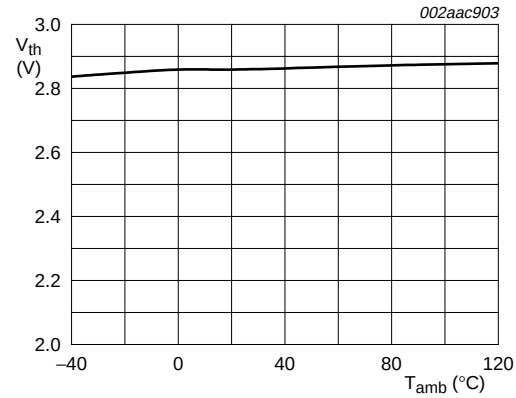
V_{DD} = 3.0 V to 3.6 V.

Fig 30. Conversion period



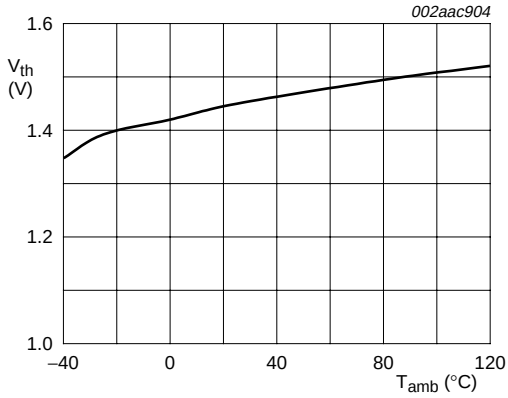
V_{DD} = 3.0 V to 3.6 V.

Fig 31. EEPROM write cycle time



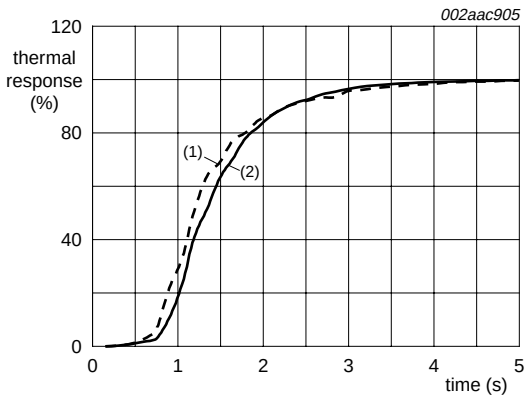
For temp sensor conversion.

Fig 32. Average power-on threshold voltage



For EEPROM read operation.

Fig 33. Average power-on threshold voltage

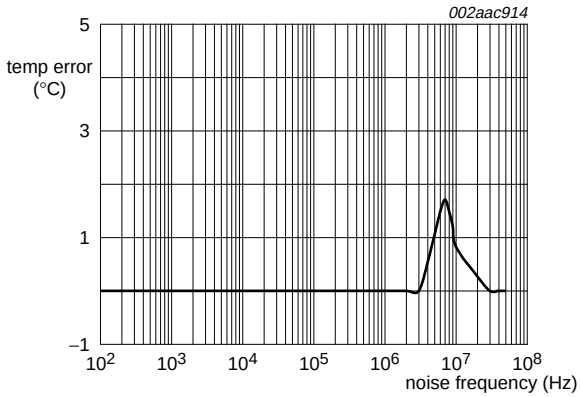


From 25 °C (air) to 120 °C (oil bath).

(1) TSSOP8

(2) HVSON8

Fig 34. Package thermal response



V_{DD} = 3.3 V + 150 mV (p-p); 0.1 µF AC coupling capacitor; no decoupling capacitor; T_{amb} = 25 °C.

Fig 35. Temperature error versus power supply noise frequency

Table 29. SMBus AC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −20 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I^2C-bus from DC to 400 kHz.

Symbol	Parameter	Conditions		V_{DD} = 1.7 V to 3.6 V		V_{DD} = 3.0 V to 3.6 V		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			-	100	-	400	kHz
t_{LOW}	LOW period of the SCL clock	10 % to 10 %		4.7	100	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	90 % to 90 %		4	-	0.6	-	µs
t_{BUF}	bus free time between a STOP and START condition		[1]	4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	10 % of SDA to 90 % of SCL	[2]	4	-	0.6	-	µs
$t_{h(Q)}$	data output hold time		[3]	300	-	300	-	ns
$t_{HD;DAT}$	data hold time		[1][8]	0	-	0	-	ns
$t_{VD;DAT}$	data valid time	from clock		200	-	200	-	ns
$t_{SU;DAT}$	data set-up time			0	-	250	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		[4]	4.7	-	0.25	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals			-	1000	-	300	ns
t_f	fall time of both SDA and SCL signals			-	300	-	300	ns
$t_{f(o)}$	output fall time			-	-	-	250	ns
$t_{to(SMBus)}$	SMBus time-out time	LOW period to reset SMBus		25	35	25	35	ms

Table 29. SMBus AC characteristics *…continued*

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −20 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I²C-bus from DC to 400 kHz.

Symbol	Parameter	Conditions	V_{DD} = 1.7 V to 3.6 V		V_{DD} = 3.0 V to 3.6 V		Unit
			Min	Max	Min	Max	
EEPROM power-up timing[5]							
$t_{pu(R)}$	read power-up time	[6]	-	1	-	1	ms
$t_{pu(W)}$	write power-up time	[6]	-	1	-	1	ms
Write cycle limits							
$T_{cy(W)}$	write cycle time	[7]	-	5	-	5	ms

[1] Delay from SDA STOP to SDA START.

[2] Delay from SDA START to first SCL HIGH-to-LOW transition.

[3] Delay from SCL HIGH-to-LOW transition to SDA edges.

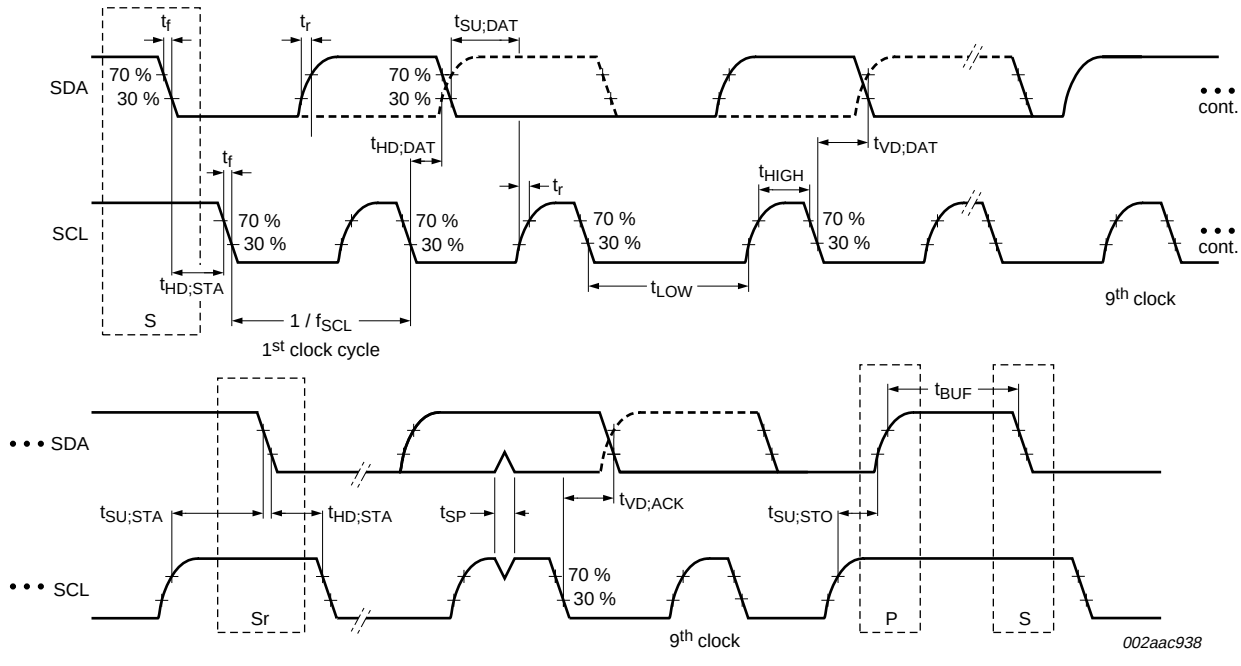
[4] Delay from SCL LOW-to-HIGH transition to restart SDA.

[5] These parameters tested initially and after a design or process change that affects the parameter.

[6] $t_{pu(R)}$ and $t_{pu(W)}$ are the delays required from the time V_{DD} is stable until the specified operation can be initiated.

[7] The write cycle time is the time elapsed between the STOP command (following the write instruction) and the completion of the internal write cycle. During the internal write cycle, SDA is released by the slave and the device does not acknowledge external commands.

[8] A device must internally provide a hold time of at least 200 ns for SDA signal (referenced to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.



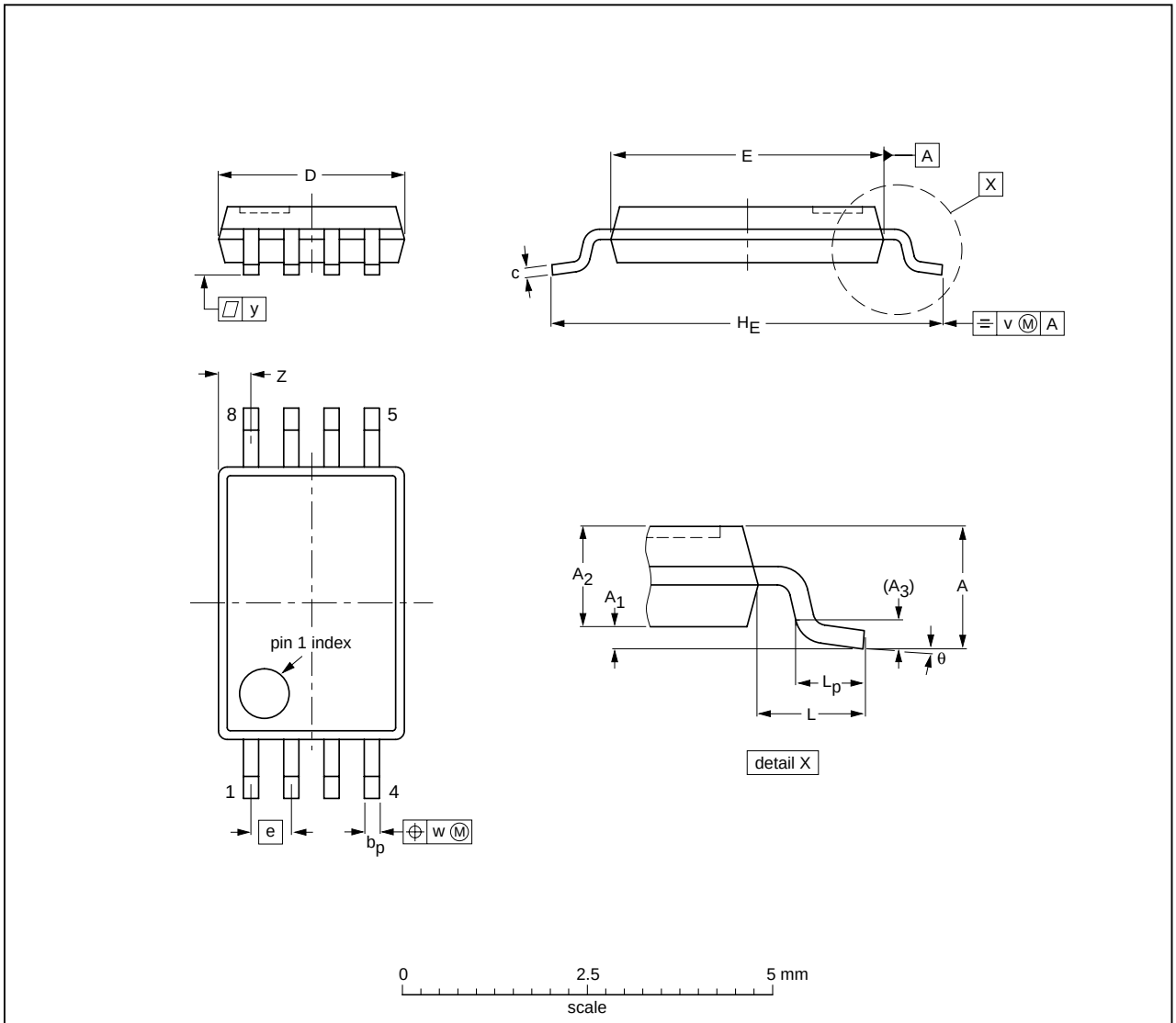
$V_{IL} = 0.3V_{DD}$

$V_{IH} = 0.7V_{DD}$

Fig 36. Definition of timing for F/S-mode devices on the I²C-bus

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

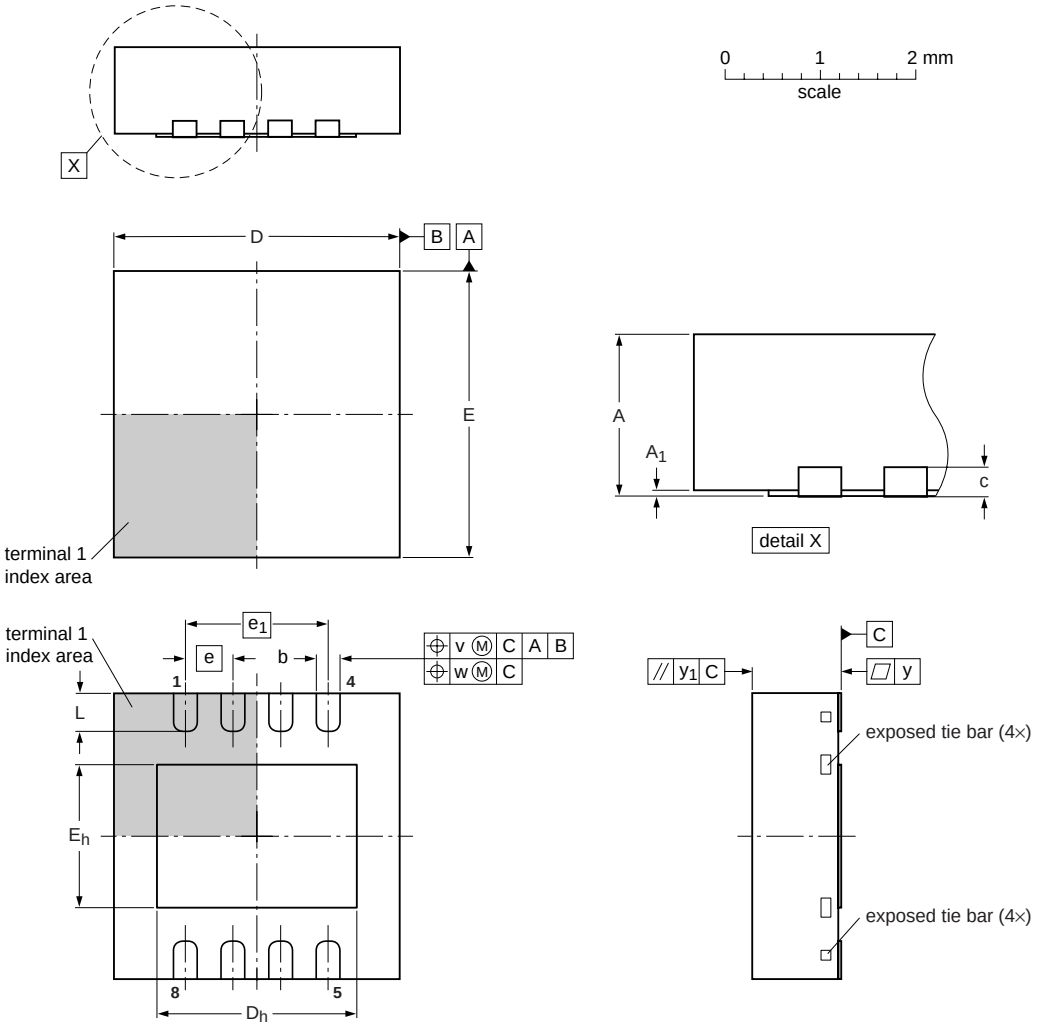
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 37. Package outline SOT530-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Fig 38. Package outline SOT908-1 (HVSON8)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 39) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 30 and 31

Table 30. SnPb eutectic process (from J-STD-020C)

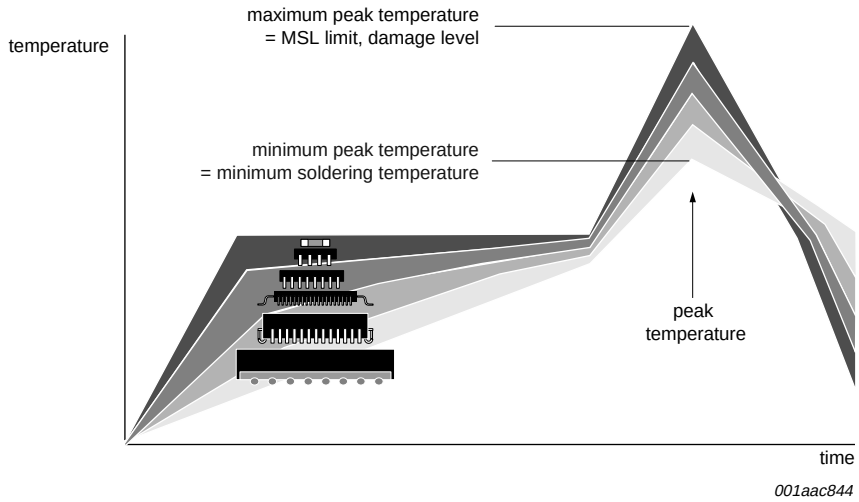
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 31. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 39.



MSL: Moisture Sensitivity Level

Fig 39. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 32. Abbreviations

Acronym	Description
ADC	A-to-D Converter
ARA	Alert Response Address
CDM	Charged Device Model
CPU	Central Processing Unit
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PC	Personal Computer
PCB	Printed-Circuit Board
POR	Power-On Reset

Table 32. Abbreviations *...continued*

Acronym	Description
SMBus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect

15. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SE97_2	20071012	Product data sheet	-	SE97_1
Modifications:	• Section 1 “General description”: – 1st paragraph, 1st sentence: changed from “provides 256-byte EEPROM of memory” to “provides 256 bytes of EEPROM memory” – 2nd paragraph, 1st sentence: changed from “Placing the Temp Sensor (TS) on DIMM” to “Placing the Temp Sensor (TS) on a DIMM” – 2nd paragraph, 2nd sentence: changed from “the ambient temperate” to “the ambient temperature” – 4th paragraph, 1st sentence: appended “using an open-drain output that can be pulled up between 0.9 V and 3.6 V“ • Table 1 “Ordering information”: topside mark for SE97TK/1 changed from “S97/1” to “97/1” • Section 7.3 “EVENT output”: added (new) 2nd paragraph • Section 7.9 “SMBus/I2C-bus interface”, 1st paragraph, 2nd sentence: changed from “is set to ‘00b’.” to “is set to ‘00h’.” • Figure 20: title modified; added “3.3 V” to topmost signal line (V_{DD}). • Added (new) Figure 21 • Table 26: removed power dissipation specification • Table 27 “Characteristics”: specifications for $I_{DD(AV)}$, $I_{sd(VDD)}$, and I_L removed from this table • Figure 27 “EVENT output current” modified • Table 28: – changed table title from “SMBus DC characteristics” to “DC characteristics” – added $I_{DD(AV)}$ specification – added $I_{sd(VDD)}$ specification – $I_{OL(sink)EVENT}$ minimum value changed from “1 mA” to “2 mA” – I_{LOH}: added “$\overline{EVENT}$” to conditions; min value changed from (blank) to “–1.0 µA”; max value changed from “-” to “+1.0 µA” – I_{LIH} conditions changed from “$V_I = V_{DD}$ or V_{SS}” to “SDA, SCL; $V_I = V_{DD}$” – I_{LIL} conditions changed from “$V_I = V_{DD}$ or V_{SS}” to “SDA, SCL; $V_I = V_{SS}$”; added condition and values for A0, A1, A2 pins – removed I_{stb} specification – added I_L specification – added I_{pd} specification • (old) Figure 35 and Figure 36 replaced with (new) Figure 36 “Definition of timing for F/S-mode devices on the I2C-bus”			
SE97_1	20070524	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contact information

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For sales office addresses, send an email to: **salesaddresses@nxp.com**

18. Contents

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